Fig. 1A

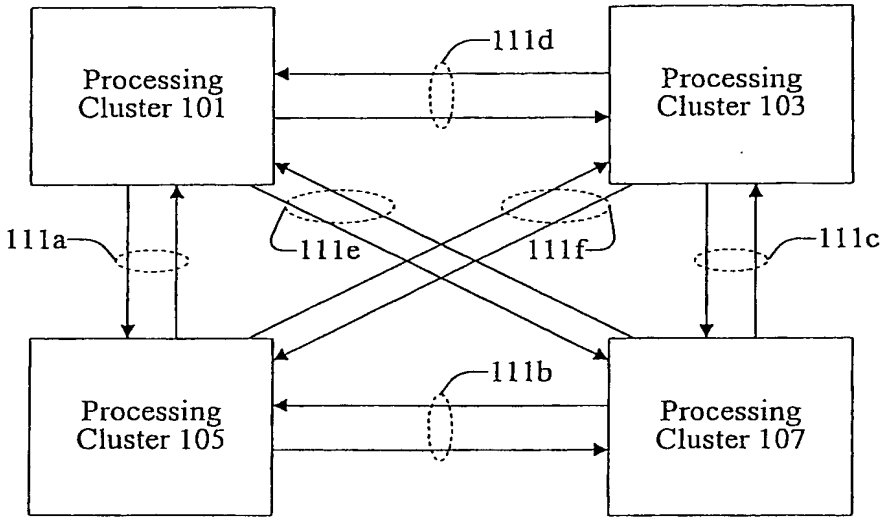

Processing Cluster 101
Processing Cluster 103
Processing Cluster 105
Processing Cluster 107
111a
111b
111c
111d
111e
111f

Fig. 1B

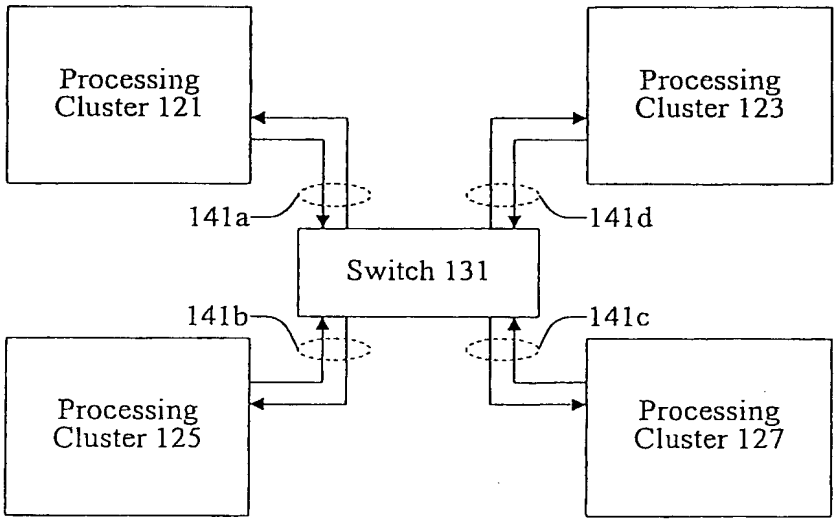
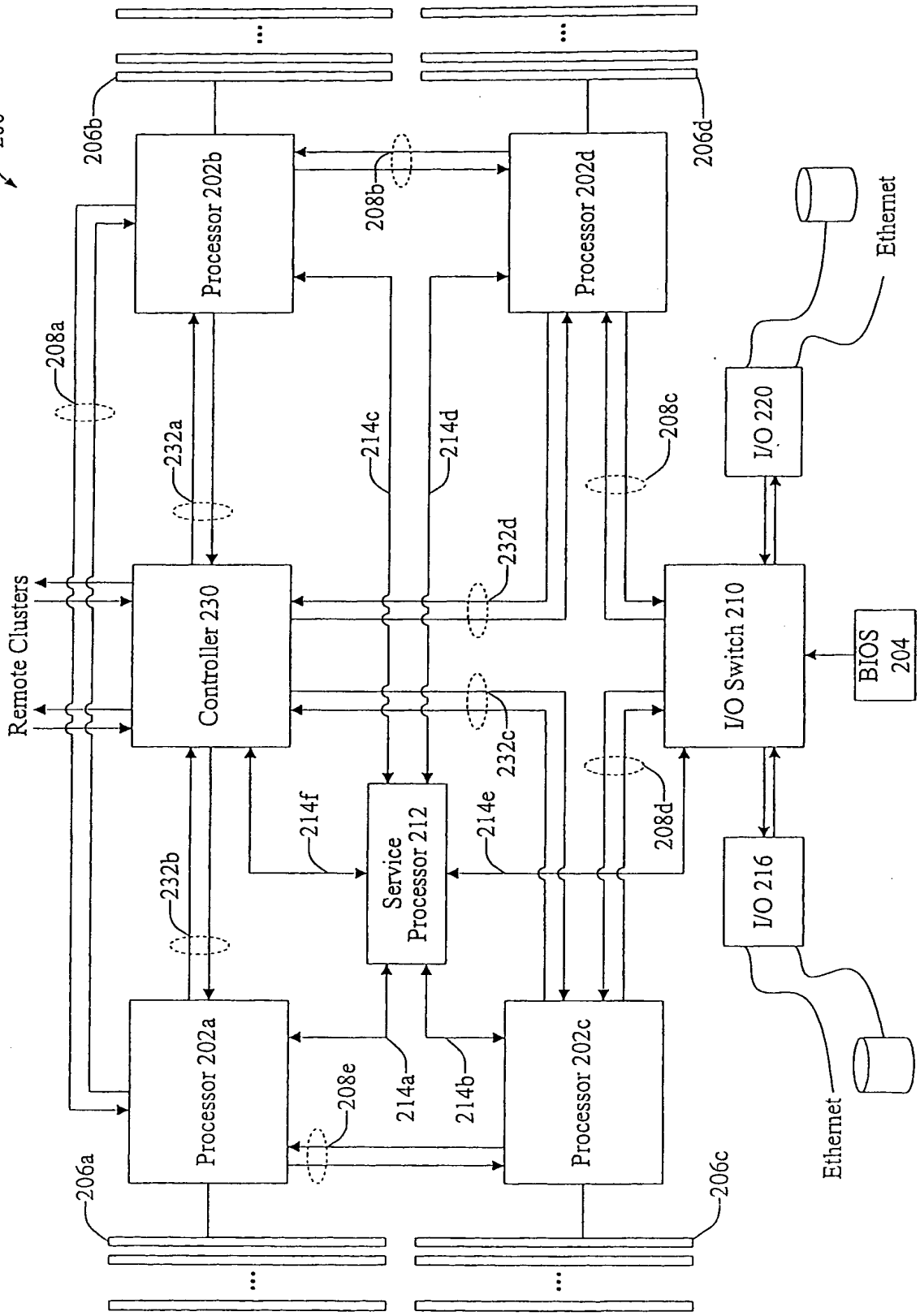

Processing Cluster 121
Processing Cluster 123
Processing Cluster 125
Processing Cluster 127
Switch 131
141a
141b
141c
141d

Fig. 2


200
206b
206d
Processor 202b
Processor 202d
208b
208a
232a
214c
214d
208c
Ethernet
I/O 220
Remote Clusters
Controller 230
232d
I/O Switch 210
BIOS 204
232c
214f
214e
208d
Service Processor 212
232b
I/O 216
Processor 202a
Processor 202c
208e
214a
214b
206a
206c
Ethernet

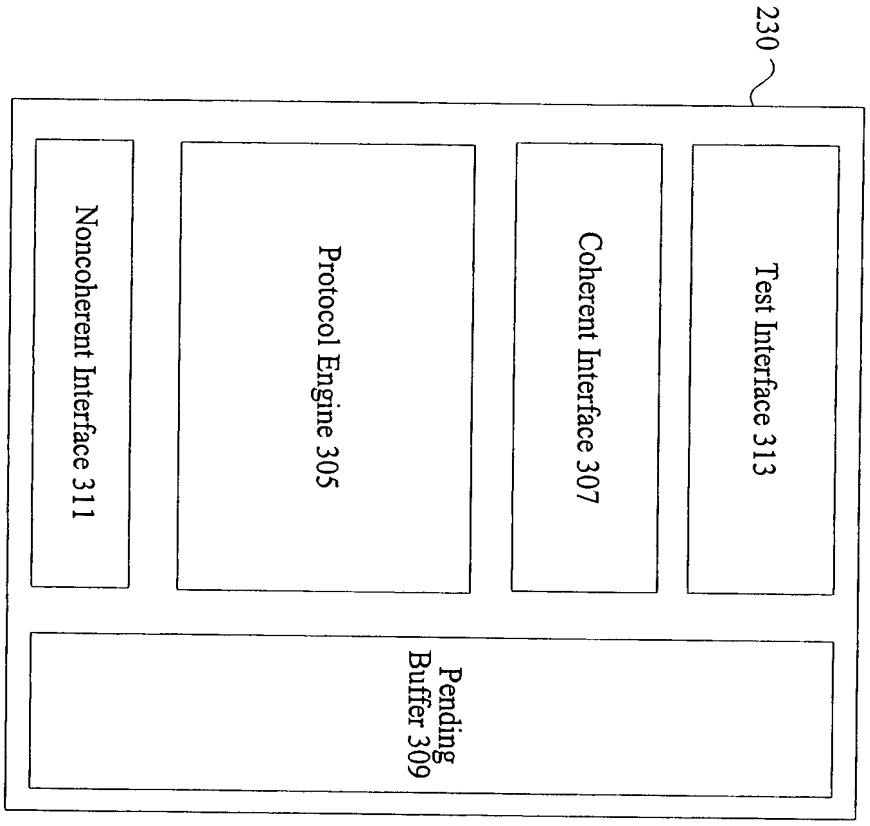

230
Test Interface 313
Coherent Interface 307
Protocol Engine 305
Noncoherent Interface 311
Pending Buffer 309

Fig. 3A

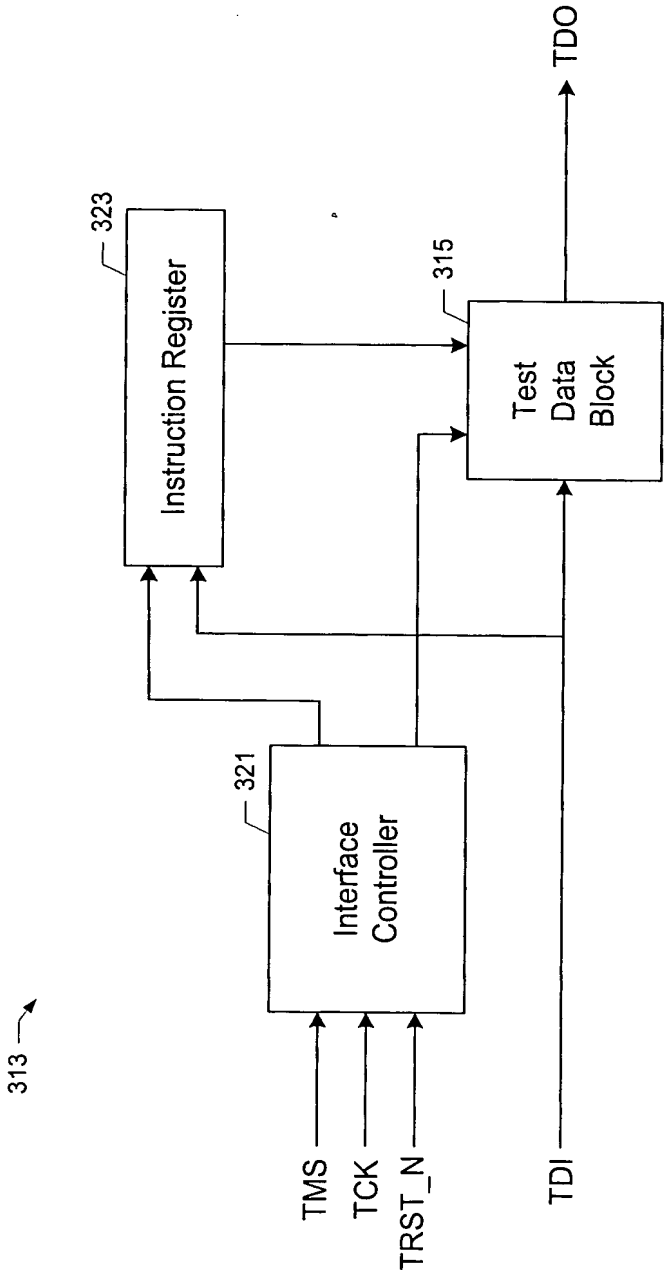

313
323
Instruction Register
315
Test Data Block
TDO
321
Interface Controller
TMS
TCK
TRST_N
TDI

Fig. 3B

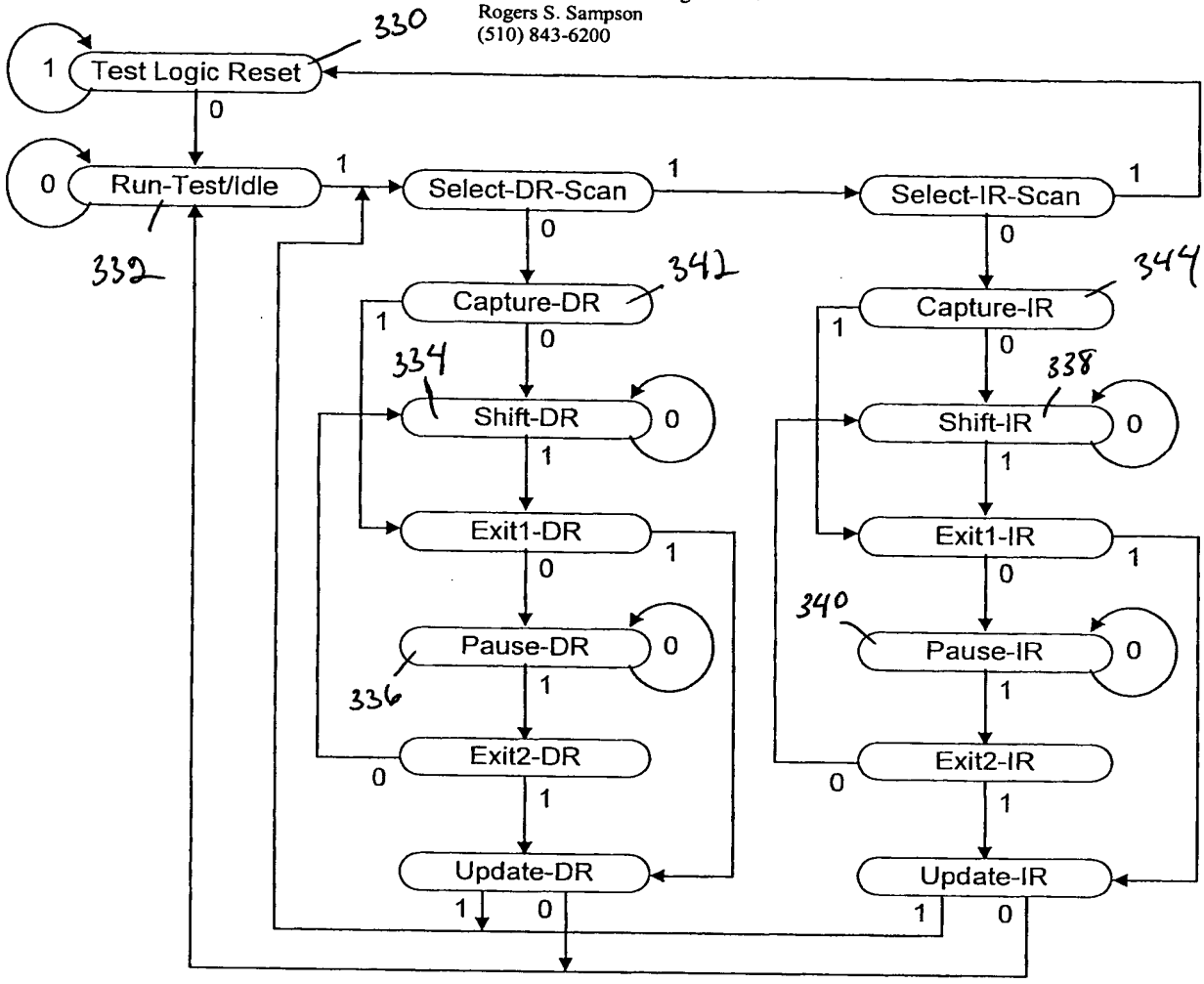

330
Test Logic Reset
Run-Test/Idle
332
Select-DR-Scan
Capture-DR
342
334
Shift-DR
Exit1-DR
Pause-DR
336
Exit2-DR
Update-DR
Select-IR-Scan
Capture-IR
344
338
Shift-IR
Exit1-IR
340
Pause-IR
Exit2-IR
Update-IR

Fig. 3C

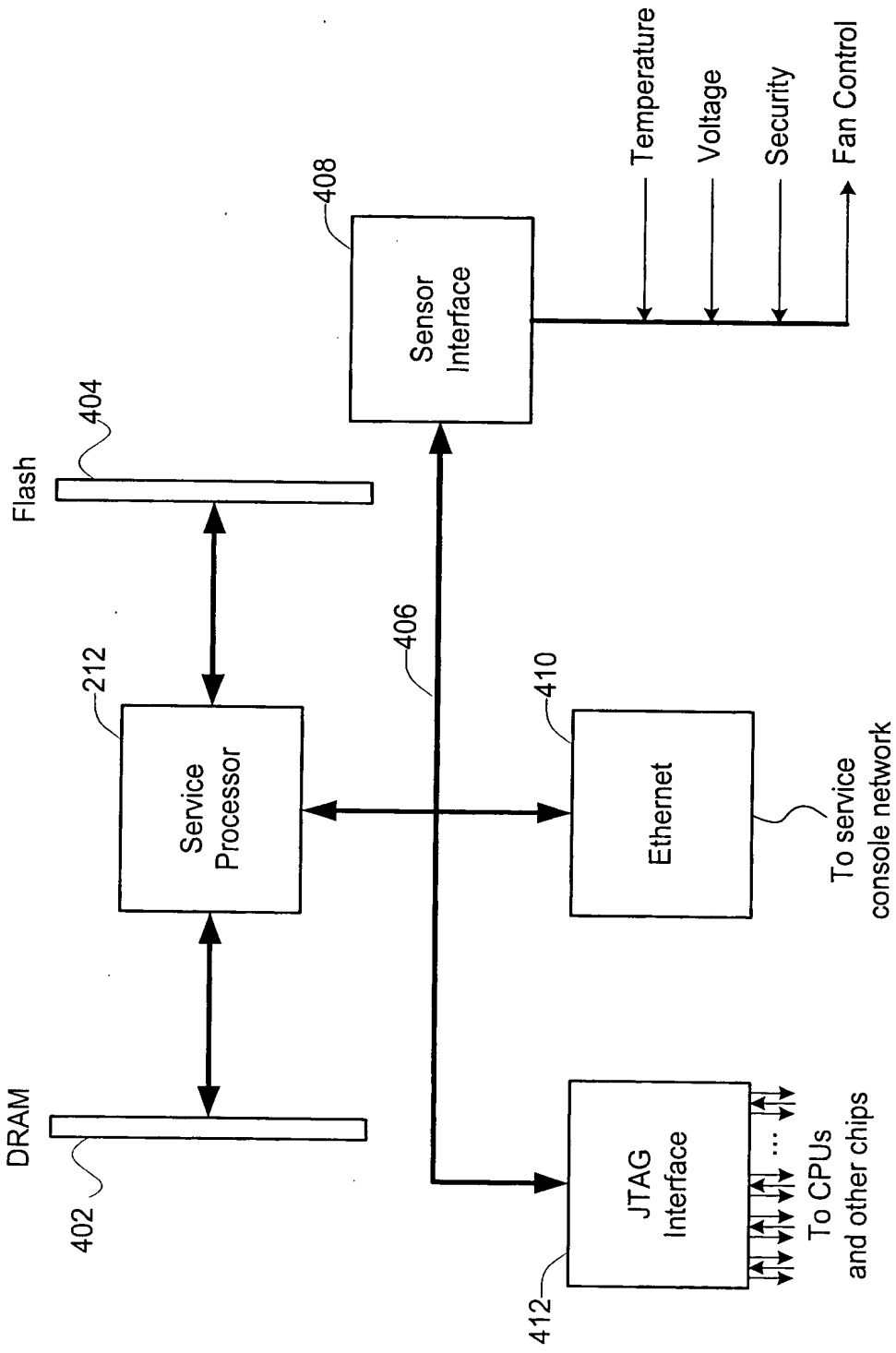

Temperature
Voltage
Security
Fan Control
408
Sensor Interface
404
Flash
406
212
Service Processor
410
Ethernet
To service console network
DRAM
402
JTAG Interface
412
To CPUs and other chips

Fig. 4A

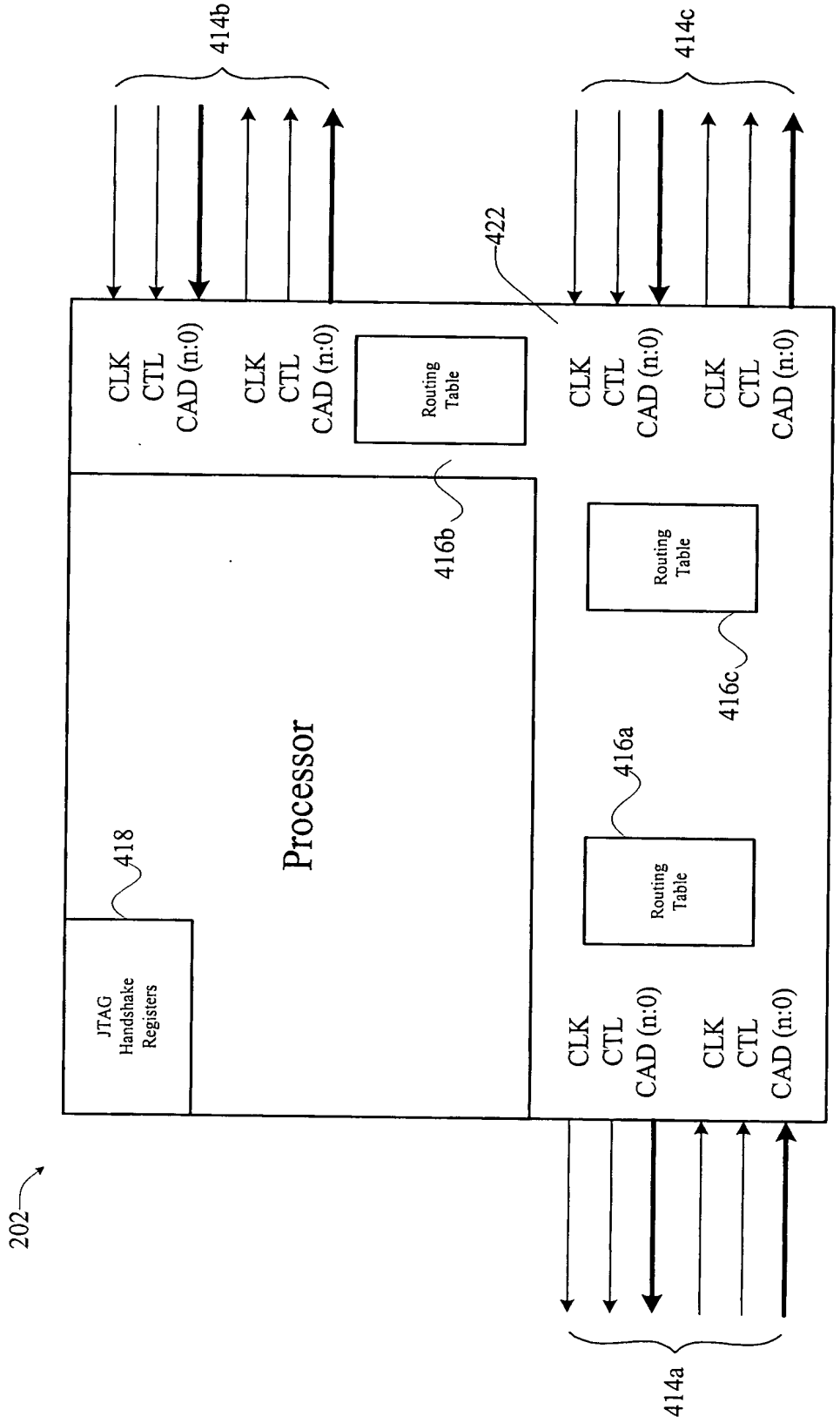

414b
414c
422
CLK
CTL
CAD (n:0)
CLK
CTL
CAD (n:0)
Routing Table
CLK
CTL
CAD (n:0)
CLK
CTL
CAD (n:0)
416b
Routing Table
416c
Processor
416a
Routing Table
418
JTAG Handshake Registers
CLK
CTL
CAD (n:0)
CLK
CTL
CAD (n:0)
202
414a

Fig. 4B

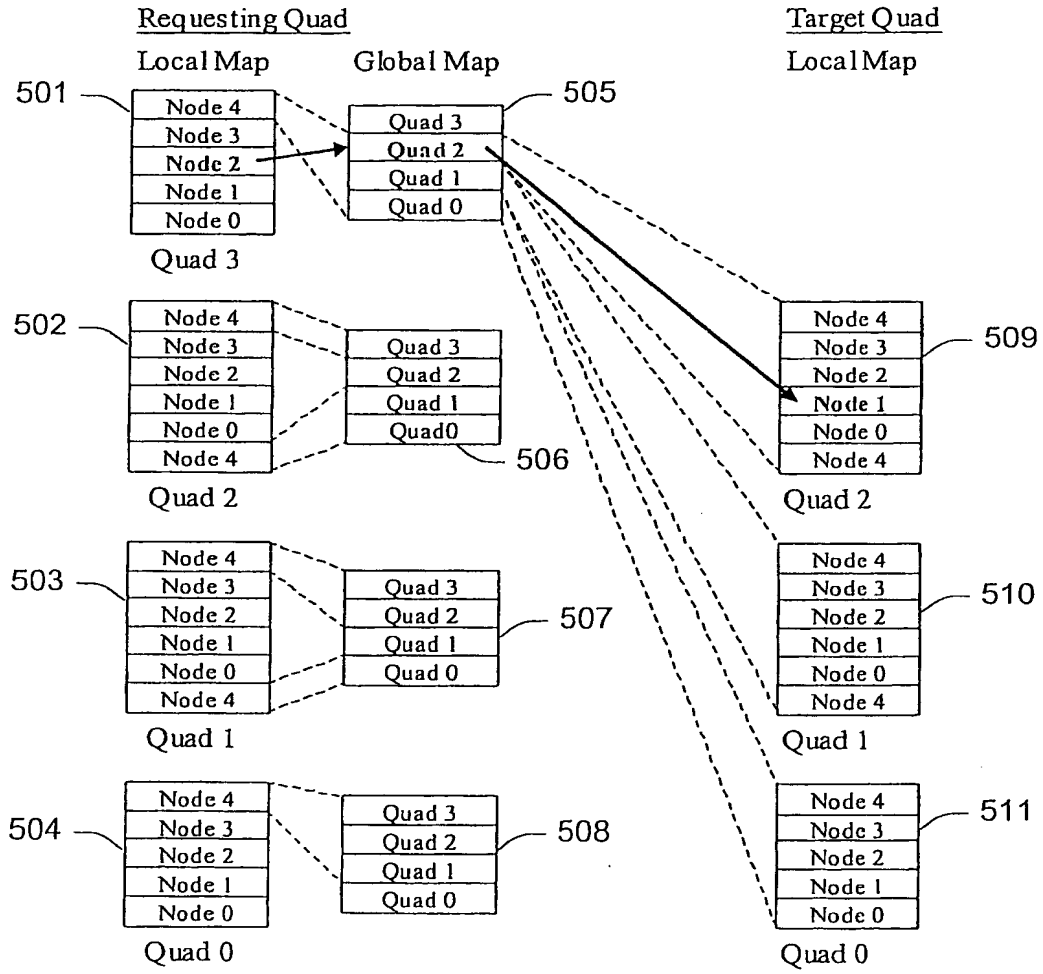

Requesting Quad
Local Map
Global Map
Target Quad
Local Map
501
Node 4
Node 3
Node 2
Node 1
Node 0
Quad 3
505
Quad 3
Quad 2
Quad 1
Quad 0
Quad 3
502
Node 4
Node 3
Node 2
Node 1
Node 0
Node 4
Quad 3
Quad 2
Quad 1
Quad0
506
Quad 2
509
Node 4
Node 3
Node 2
Node 1
Node 0
Node 4
Quad 2
503
Node 4
Node 3
Node 2
Node 1
Node 0
Node 4
Quad 3
Quad 2
Quad 1
Quad 0
507
Quad 1
510
Node 4
Node 3
Node 2
Node 1
Node 0
Node 4
Quad 1
504
Node 4
Node 3
Node 2
Node 1
Node 0
Quad 3
Quad 2
Quad 1
Quad 0
508
Quad 0
511
Node 4
Node 3
Node 2
Node 1
Node 0
Quad 0

Fig. 5

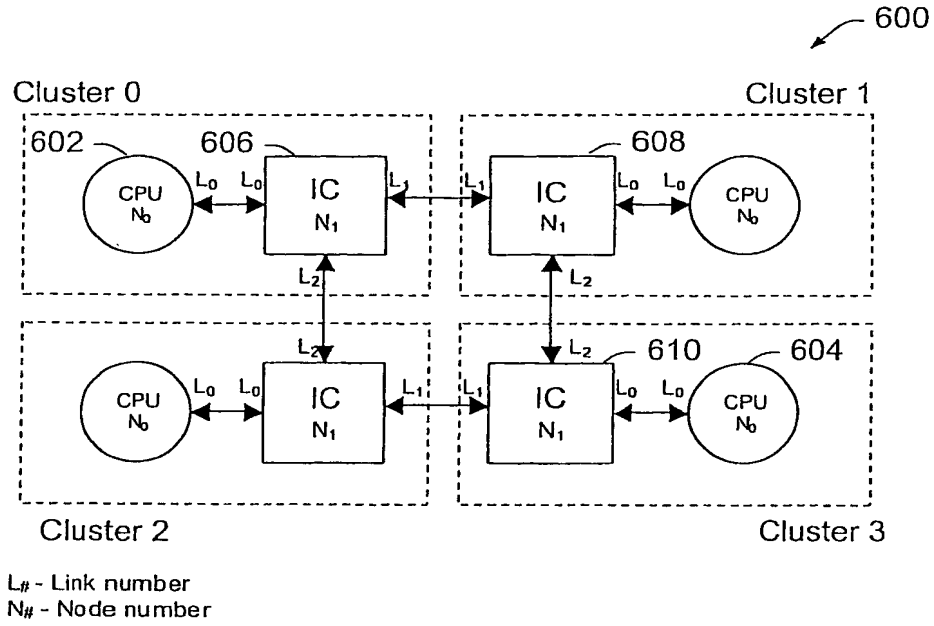


Fig. 6A

		Local Table		Global Table			
		Dest Node		Dest Cluster			
Source		N_0	N_1	C_0	C_1	C_2	C_3
Cluster 0	Node 0	X	L_0	NA	NA	NA	NA
	Node 1	L_0	X	X	L_1	L_2	L_1
Cluster 1	Node 0	X	L_0	NA	NA	NA	NA
	Node 1	L_0	X	L_1	X	L_2	L_2
Cluster 2	Node 0	X	L_0	NA	NA	NA	NA
	Node 1	L_0	X	L_2	L_2	X	L_1
Cluster 3	Node 0	X	L_0	NA	NA	NA	NA
	Node 1	L_0	X	L_2	L_2	L_1	X

Fig. 6B

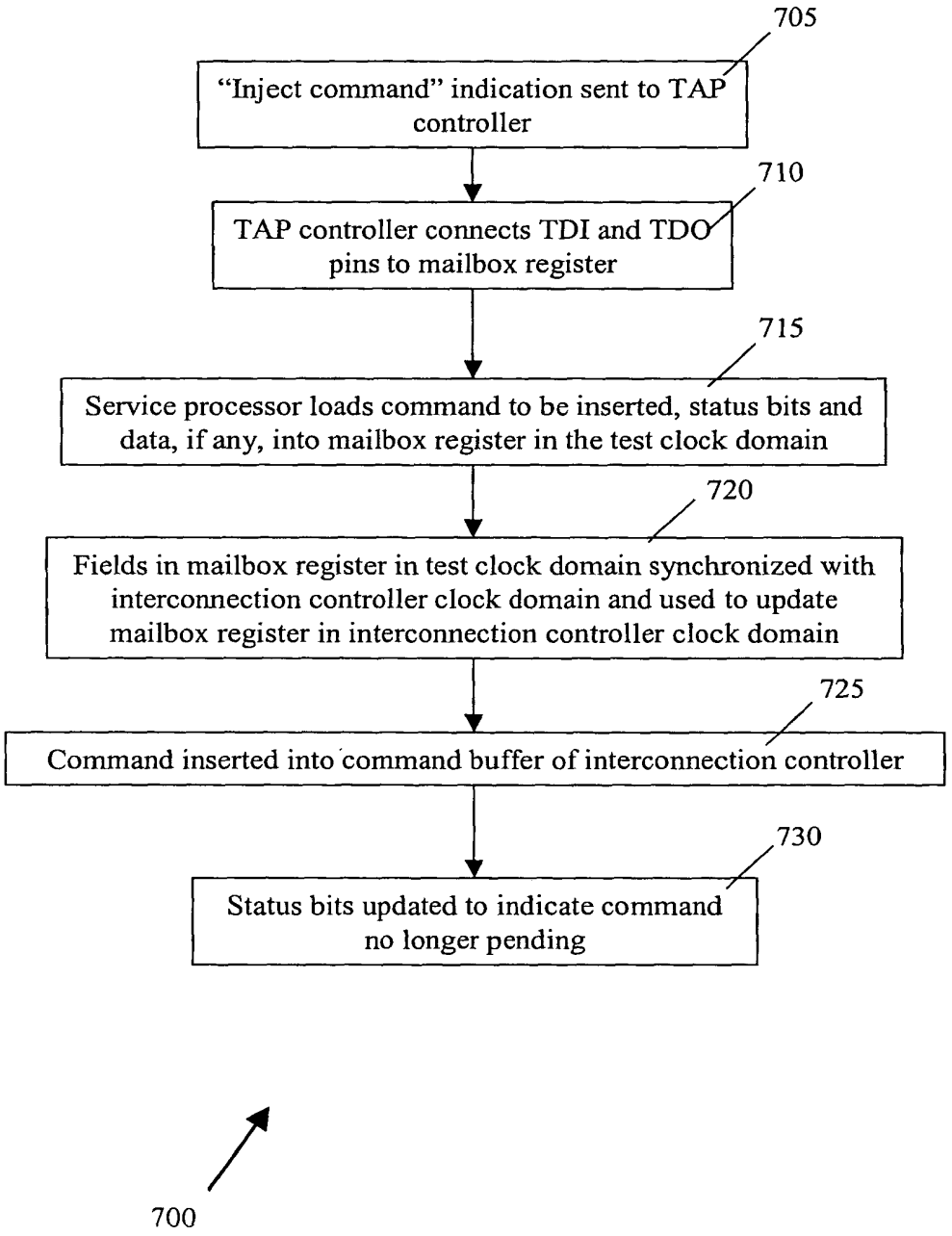

705
"Inject command" indication sent to TAP controller
710
TAP controller connects TDI and TDO pins to mailbox register
715
Service processor loads command to be inserted, status bits and data, if any, into mailbox register in the test clock domain
720
Fields in mailbox register in test clock domain synchronized with interconnection controller clock domain and used to update mailbox register in interconnection controller clock domain
725
Command inserted into command buffer of interconnection controller
730
Status bits updated to indicate command no longer pending
700

Fig. 7

	Name	Description
805	HT Data	Data Associated with the Mailbox HT Command
810	DataValid	Valid bit for each double word (DW) of HT data
815	RCV LINK ID	Indicates the ID of link on which the packet was received.
820	XMT LINK SEL	Transmit Link Selector.
825	DATA PTRV	Data Pointer Valid. Indicates that the Mailbox HT Command has data associated with it.
830	DATA PTR	Data Pointer.
835	REM Link Ext	Remote Link Extension Bits. Contains information pertaining to remote links such as QUAD_ID etc.
840	HT CMD	64-bit HT Command.
845	SPJTAG_CMD	Command issued to the SPJTAG Unit. A non-zero value in this field causes the HT CMD field to be ignored.
850	NRE	No Response Expected. Indicates that no response is to be expected for the HT command shifted in. When set, it causes the Fbit to be set as soon as the command is accepted.
855	FRC	Force Command Bit. When set, the supplied command is forced into the system ignoring the Finished status bit.
860	PRIO	Priority Command Bit. Set by software to indicate that the HT Command needs to be sent to the CAR directly. This bit should be set only for Configuration RD/WR HT Commands to the local Horus.
865	P_bit	Command Pending Bit. Set by software to indicate that there is a new command shifted into the mailbox register.
870	F_bit	Finished Bit. Set by Horus on completing the HT command. Indicates that the response to the command is ready to be captured from the Horus mailbox register.

800

Fig. 8

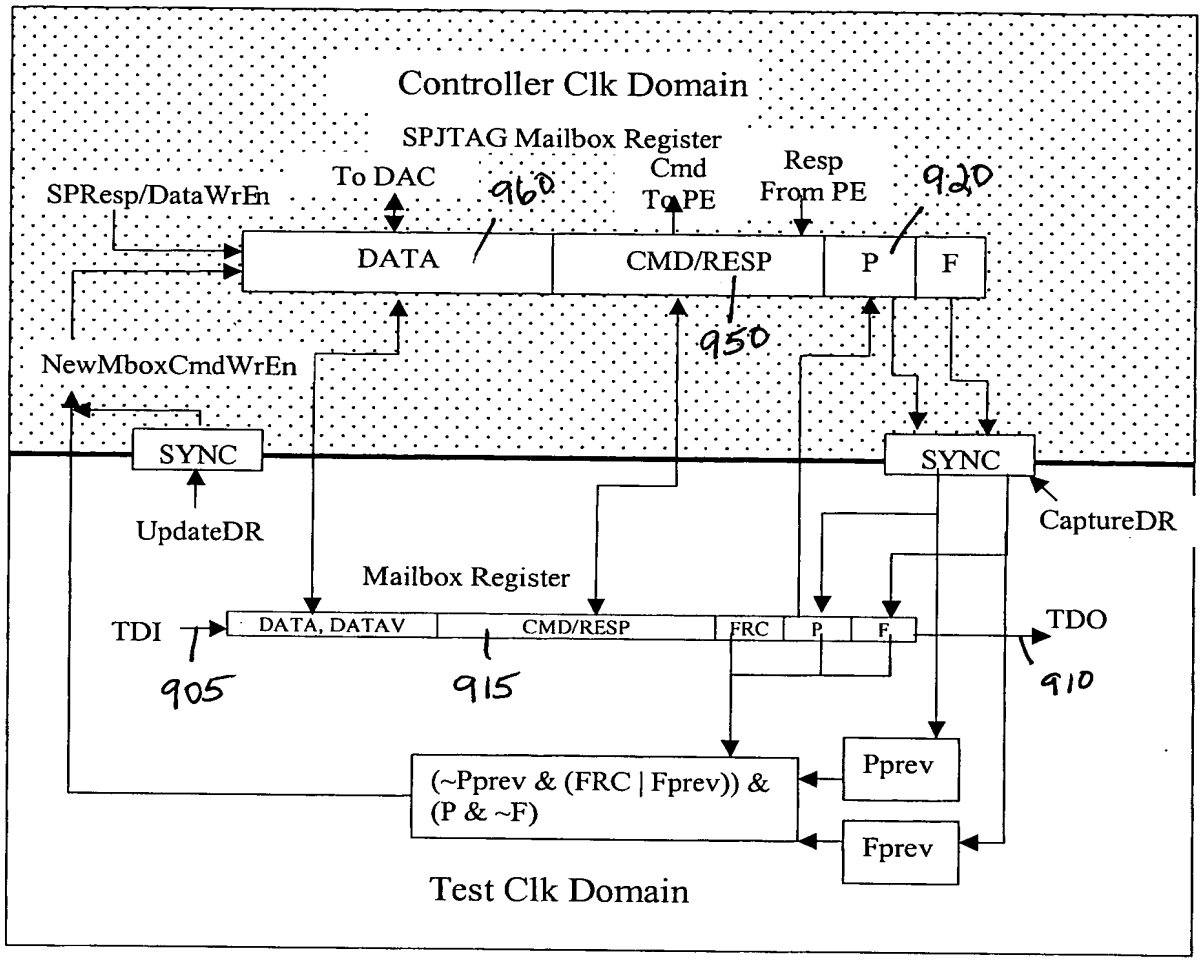

Controller Clk Domain
SPJTAG Mailbox Register
To DAC
960
Cmd
To PE
Resp
From PE
920
SPResp/DataWrEn
DATA
CMD/RESP
P
F
950
NewMboxCmdWrEn
SYNC
SYNC
UpdateDR
CaptureDR
Mailbox Register
TDI
DATA, DATAV
CMD/RESP
FRC
P
F
TDO
905
915
910
(~Pprev & (FRC | Fprev)) &
(P & ~F)
Pprev
Fprev
Test Clk Domain

Fig. 9

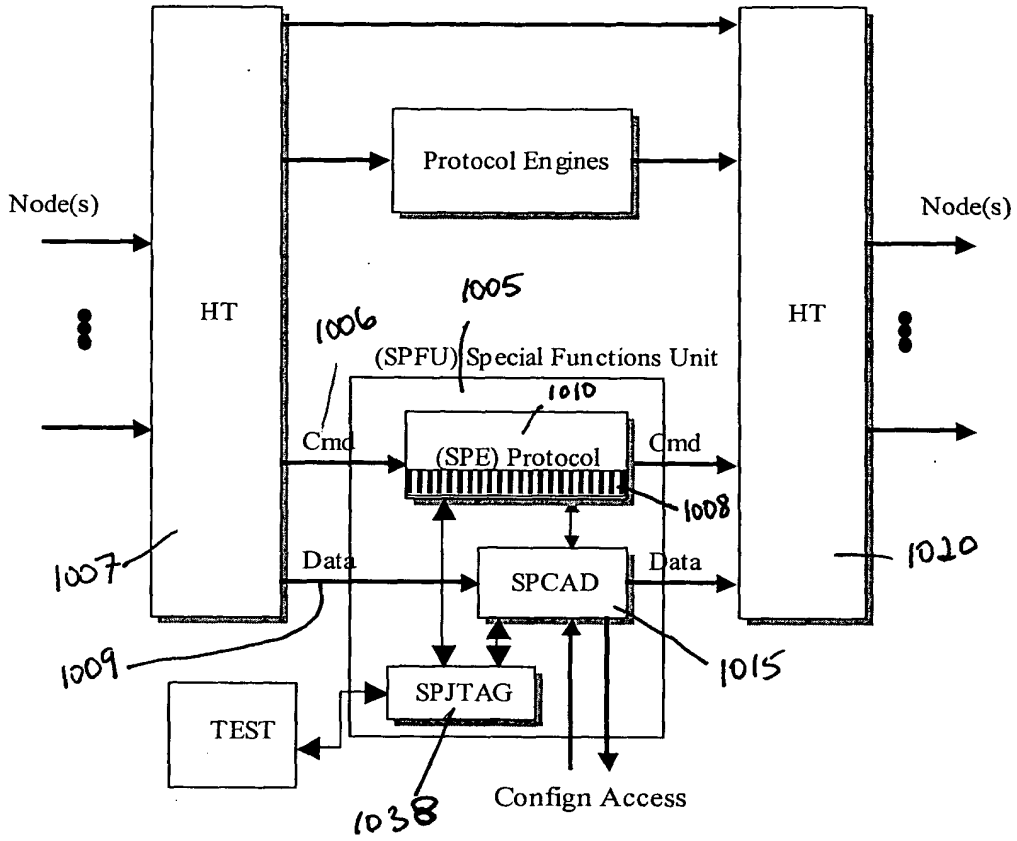

Node(s)
HT
Protocol Engines
HT
Node(s)
1005
1006
(SPFU) Special Functions Unit
1010
Cmd
(SPE) Protocol
Cmd
1008
1007
Data
SPCAD
Data
1020
1009
1015
SPJTAG
TEST
1038
Confign Access

Fig. 10